UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/758,033	01/16/2004	Kunio Kanda	392.1861	6141

21171 7590 12/08/2005

STAAS & HALSEY LLP
SUITE 700
1201 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
ZAMAN, FAISAL M	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 12/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/758,033	KANDA ET AL.	
	Examiner	Art Unit	
	Faisal Zaman	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/16/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The references listed on the Information Disclosure Statement submitted on 16 January 2004 have been considered by the examiner (see attached PTO-1449).

Claim Objections

2. Claim 6 is objected to because of the following informalities: In Line 1, "The method" should read "A method", since it is an independent claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claims 1-6** are rejected under 35 U.S.C. 102(b) as being anticipated by Sone et al. ("Sone") (U.S. Patent No. 5,524,217).

Regarding Claim 1, Sone discloses a device for transmitting wired OR signal between two systems (abstract), each system comprising:

Output means for switching between a first state in which the system outputs a signal state of the wired OR signal line and a second state in which the system outputs

a negate state of the wired OR signal line (Column 13, lines 44-56), and outputting either state to the other system (abstract, Column 22, lines 24-36);

Switching control means for switching an output state of said output means (Column 12, lines 16-38); and

An assert mechanism that maintains the wired OR signal line in an asserted state in response to an asserted state transferred by the output means of the other system (Column 14, lines 1-18).

Regarding Claim 2, Sone discloses wherein said switching control means comprises a register controlled by a processor in the system (abstract, Column 3, lines 28-32), and said output means comprises:

A mask mechanism which switches to said first state when the register indicates a predetermined value and which switches to the second state when the register indicates another value (Figure 23, items 46a and 54, Column 13, lines 7-67); and

A transmission mechanism that transfers an output from said mask mechanism to the other system (Figure 23, item 49, Column 13, lines 31-34).

Regarding Claim 3, Sone discloses a device for transmitting wired OR signal between two systems (abstract), each system comprising:

Output means for outputting the signal state of a wired OR signal line to the other system (abstract, Column 22, lines 24-36);

Switching and outputting means for switching between the first state where the signal state transmitted by the output means in the other system is output and the second state where negate state is output, and outputting the switched state (Column 13, lines 44-56);

Switching and controlling means for switching the output of said switching and outputting means (Column 12, lines 16-38); and

An assert mechanism that switches the wired OR signal line between an asserted state or a negate state according to the output state of said switching and outputting means (Column 14, lines 1-18).

Regarding Claim 4, Sone discloses wherein said switching and controlling means is composed of a register controlled by a processor in the system (abstract, Column 3, lines 28-32), and said switching and outputting means is composed of a mask mechanism which switches to the first state when said register has a predetermined value and switches to the second state when the register has a value other than the predetermined value (Figure 23, items 46a and 54, Column 13, lines 7-67).

Regarding Claim 5, Sone discloses a method for communicating wired OR signal between two systems (abstract), in which each system comprises output means for switching between a first state in which the system outputs a signal state of the wired OR signal line and a second state in which the system outputs a negate state of the

wired OR signal line (Column 13, lines 44-56), and outputting either state to the other system (abstract, Column 22, lines 24-36), and assert means for maintaining the wired OR signal line in the system in an asserted state in response to an assert signal from the output means of the other system (Column 14, lines 1-18), the method comprising:

switching the wired OR signal line in one of the systems to the asserted state if the wired OR signal line of one of the systems is brought into the asserted state, when each of the output means is in the first state (Column 12, lines 16-38);

processing a device that has brought the wired OR signal line in said other system into the asserted state, after the switching (Column 10 lines 33 – Column 11 line 4, executing a corresponding interrupt service routine in Sone is considered equivalent to processing a device in the current application); and

switching each of said output means to the second state, verifying the negate state of the wired OR signal lines in the two systems, and then switching each of said output means to the first state, after finishing the processing of the device (Column 11 line 64 – Column 12 line 38, the acknowledgement signal in Sone is considered equivalent to the verification of the negate state as described in this limitation).

Regarding Claim 6, Sone discloses the method for transmitting wired OR signal between two systems (abstract), in which each system comprises output means for outputting the signal state of a wired OR signal line to the other system (abstract, Column 22, lines 24-36); switching and outputting means for switching between the first state where the signal state transmitted by the output means in the other system is

output and the second state where negate state is output, and outputting the switched state (Column 13, lines 44-56); switching and controlling means for switching the output of said switching and outputting means (Column 12, lines 16-38); and an assert mechanism that switches the wired OR signal line between an asserted state or a negate state according to the output state of said switching and outputting means (Column 14, lines 1-18); the method comprising:

switching the wired OR signal line in one of the two systems to the asserted state if the wired OR signal line of the other system is brought into the asserted state, when each of the switching and outputting means is in the first state (Column 12, lines 16-38);

processing a device that has brought the wired OR signal line in said other system into the asserted state, after the switching (Column 10 lines 33 – Column 11 line 4); and

switching each of said switching and outputting means to the second state, verifying the negate state of the wired OR signal lines in the two systems, and then switching each of said switching and outputting means to the first state, after finishing the processing of the device (Column 11 line 64 – Column 12 line 38).

Prior Art of Record

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Nishioka (U.S. Patent No. 4,799,148) discloses an interrupt control system having a processor for determining service priority among a plurality of modules according to an interrupt status table. D'Amico et al. (U.S. Patent No.

4,796,176) discloses a method of interrupt handling in a dual processor system. Sarangdhar et al. (U.S. Patent No. 5,659,689) discloses a method and apparatus for transmitting information on a wired-or bus. Kumar et al. (U.S. Patent Publication No. 2002/0087765) discloses a method and system for completing purge requests or the like in a multi-node multiprocessor system. Delvaux (U.S. Patent No. 6,608,571) discloses a system and method for communicating over a one-wire bus. Friel et al. (U.S. Patent No. 6,697,897) discloses a data communication interface between host and slave processors. Sakaue (U.S. Patent No. 6,754,205) discloses a switching element and packet switch. Jurasek et al. (U.S. Patent No. 6,954,451) discloses a distributed time-multiplexed bus architecture and emulation apparatus.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Faisal Zaman whose telephone number is 571-272-6459. The examiner can normally be reached on Monday thru Friday, 9 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

fmz

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
12/5/05